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09/771,718	01/30/2001	Kenji Numata	045054/0135	9477

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EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2122	9

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/771,718	NUMATA, KENJI	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5,7,8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-31 are pending and have been examined. The priority date considered for the application is 31 January 2000.

Information Disclosure Statement

2. Regarding the Information Disclosure Statement filed on 19 June 2003 (Paper No. 7), Document No. A1 has not been considered because no English translation or equivalent has been provided.

Specification

3. The disclosure is objected to because it contains grammatical informalities. The application appears to be a literal translation into English from a foreign document and is not always clear and concise. See, for example, page 1, line 25, "from an outside or an inside," which should be replaced with --from outside or inside--. See also, for example, the sentence starting on page 20, line 22, and ending on page 21, line 9, which is lengthy and unclear. Also note that "or a like" as used, for example, on page 23, line 10, should be replaced with --or the like--. Furthermore, in the title of the application, the phrase "and program development program" is redundant and could be deleted. Applicant is respectfully asked for cooperation in finding and correcting all such grammatical informalities.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

For purposes of compact prosecution, the claims have been interpreted and treated accordingly below.

Claim Rejections - 35 USC § 102

6. It is noted that claims 1-31 are anticipated by Japanese Unexamined Patent Application Publication H06-175844 and Republic of Korea Registered Utility Model Publication 0076805, as shown in the Information Disclosure Statement filed on 19 June 2003 (Paper No. 7). The translated portion of the Korean Office Action shows that the cited inventions are "extremely similar to the invention of the present application in terms of constitution and effect, with other differences in constitution being no more than matters of choice which could be selectively adopted as necessary by a person skilled in the art or easily achieved by simple circuit modification." As further shown, "no difficulty of constitution is found, and thus the invention of the present application could have been easily invented by a person having ordinary knowledge in the relevant technical field."

Cooperation is respectfully asked of applicant to provide full English translations of the foreign documents or an explanation as to how the present invention is not anticipated by the cited references.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,141,791 to Takuma et al. (hereinafter Takuma) in view of U.S. Pat. No. 5,828,829 to Yamauchi et al. (hereinafter Yamauchi).

With respect to claim 1, Takuma discloses a program development apparatus used for developing a program to be installed in a system having at least a first central processing and an other component (see Fig. 2B, which shows a compiler and a debugger for program development on a system having a host processor and other components).

Takuma further discloses a program generating section for generating said program (see Fig. 11, which shows a compiler for generating the program), but does not show an event pseudo-generating routine for pseudo-generating said event based on a state-transition matrix and event pseudo-generating information for pseudo-generating a same event as an event which normally occurs based on data or a signal transmitted from said other component to said first central processing unit in said system, wherein said state-transition matrix has a plurality of cells, each of said cells defined by a state in which said system to be a subject of a program development is enabled to be and an event which is an impulse from an outside or an inside of said system and further wherein a content of a process to be executed by said system and a state

of a transition destination to be transited when a corresponding event occurs under a corresponding state are described in each said cell.

Yamauchi shows the features above in a software development system used for testing programs (see the abstract). Yamauchi discloses causing or generating events based on state transitions (see column 4, lines 44-48; see also column 3, lines 21-45, which shows that events are internal or external signals sent from a component to the processor) and a state transition table or matrix that includes start and end states, events, and actions to be taken (see Fig. 3 and column 9, lines 31-39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

Takuma further discloses a second central processing unit having a same function as said first central processing unit and for executing emulation of said program and said event pseudo-generating routine (see Fig. 2B and column 8, lines 5-12, which shows an in-circuit emulator having a processor for performing the same functions as a first processor).

Takuma does not show an analysis section for starting said emulation of said program from a state input as an initial state and for referring to said pseudo-generating information and rewriting information for pseudo-generating said event memorized in a memory section used in executing said event pseudo-generating routine into information corresponding to said event which is instructed to occur.

Takuma does show emulating the program (see column 13, lines 54-63).

Yamauchi discloses the features above in terms of defining a state transition model for a program having an initial state (see column 9, lines 11-25), and defining a test sequence comprising transition information for causing events, organized in data structures stored in memory (see column 9, lines 48-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

With respect to claim 2, Takuma discloses a program development apparatus used for developing a program to be installed in a system having at least a first central processing and an other component (see Fig. 2B, which shows a compiler and a debugger for program development on a system having a host processor and other components).

Takuma does not disclose:

(a) a state-transition matrix memory section for memorizing a state-transition matrix, wherein said state-transition matrix has a plurality of cells, each of said cells defined by a state in which said system to be a subject of a program development is enabled to be and an event which is an impulse from an outside or an inside of said system and further wherein a content of a process to be executed by said system and a state of a transition destination to be transited when a corresponding event occurs under a corresponding state are described in each said cell.

(b) an event pseudo-generating editor for generating event pseudo-generating information for pseudo-generating a same event as an event which normally occurs based on data or a signal transmitted from said other component to a first central processing unit in said system.

Yamauchi discloses the features of (a) above in terms of a state transition table or matrix that includes start and end states, events, and actions to be taken (see Fig. 3 and column 9, lines 31-39; see also column 3, lines 21-45, which shows that events are internal or external signals sent from a component to the processor), which is stored in an area allocated in memory (see column 9, lines 23-30).

Yamauchi further discloses the features of (b) above in terms of an editor for defining a state transition model comprising events and actions (see Fig. 2 and column 9, lines 11-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

Takuma further discloses a program generating section for generating said program (see Fig. 11, which shows a compiler for generating the program), but does not show an event pseudo-generating routine for pseudo-generating said event.

Yamauchi further discloses the features above in terms of generating events based on state transitions (see column 4, lines 44-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the

purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

Takuma further discloses a second central processing unit for having a same function as said first central processing unit and for executing emulation of said program and said event pseudo-generating routine (see Fig. 2B and column 8, lines 5-12, which shows an in-circuit emulator having a processor for performing the same functions as a first processor).

Takuma does not disclose:

(c) an input section for detecting which display position of each event or each state is indicated among a plurality of events and a plurality of states forming said state-transition matrix displayed on a display section and for outputting position information of said display position.

(d) an analysis section for converting said position information into an event code or a state code corresponding to said position so as to set a state corresponding to said state code as an initial state for starting emulation of said program and for referring to said pseudo-generating information so as to rewrite information memorized in a memory section used in executing said pseudo-generating routine, said information for pseudo-generating an event into information corresponding to said event code.

Yamauchi further discloses the features of (c) above in terms of an input interface for defining and displaying a sequence of state transitions and events (see Figs. 4, 6 and 8) and a state table or matrix having coordinates for a display position (see column 9, lines 26-30).

Yamauchi further discloses the features of (d) above in terms of converting a state transition model describing events and actions into a data structure, stored in memory, having event and state identification codes (see Fig. 3 and column 9, lines 11-39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

With respect to claim 3, Takuma discloses a program development apparatus used for developing a program to be installed in a system having at least a first central processing and an other component (see Fig. 2B, which shows a compiler and a debugger for program development on a system having a host processor and other components).

Takuma does not disclose:

(a) a state-transition matrix memory section for memorizing a state-transition matrix, wherein said state-transition matrix has a plurality of cells, each of said cells defined by a state in which said system to be a subject of a program development is enabled to be and an event which is an impulse from an outside or an inside of said system and further wherein a content of a process to be executed by said system and a state of a transition destination to be transited when a corresponding event occurs under a corresponding state are described in each said cell.

(b) an event pseudo-generating editor for generating event pseudo-generating information for pseudo-generating a same event as an event which normally occurs based on data or a signal transmitted from said other component to a first central processing unit in said system.

Yamauchi discloses the features of (a) above in terms of a state transition table or matrix that includes start and end states, events, and actions to be taken (see Fig. 3 and column 9, lines 31-39; see also column 3, lines 21-45, which shows that events are internal or external signals sent from a component to the processor), which is stored in an area allocated in memory (see column 9, lines 23-30).

Yamauchi further discloses the features of (b) above in terms of an editor for defining a state transition model comprising events and actions (see Fig. 2 and column 9, lines 11-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

Takuma further discloses a program generating section for generating said program (see Fig. 11, which shows a compiler for generating the program), but does not show an event pseudo-generating routine for pseudo-generating said event.

Yamauchi further discloses the features above in terms of generating events based on state transitions (see column 4, lines 44-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

Takuma further discloses a second central processing unit for having a same function as said first central processing unit and for executing emulation of said program and said event pseudo-generating routine (see Fig. 2B and column 8, lines 5-12, which shows an in-circuit emulator having a processor for performing the same functions as a first processor).

Takuma does not disclose:

(c) an input section for detecting which display position of each event or each state is indicated among a plurality of events and a plurality of states forming said state-transition matrix displayed on a display section so as to output position information of said display position and for generating an input event log including an order of instructed events and an instruction timing of each event.

(d) a script generating section for generating a script file in which an occurrence timing of each event and a timing at which an element in said system operates in accordance with a specification are descried based on said input event log.

(e) a script analysis section for sequentially outputting position information of each event described in said script file and of a corresponding display area in said state-transition matrix displayed on said display section in order and at an occurrence timing described in said script file.

(f) an analysis section for converting said position information into an event code or a state code corresponding to said position so as to set a state corresponding to said state code as an initial state for starting emulation of said program and for referring to said pseudo-generating information so as to rewrite information memorized in a memory section used in executing said

pseudo-generating routine, said information for pseudo-generating an event into information corresponding to said event code.

Yamauchi further discloses the features of (c) above in terms of an input interface for defining and displaying a sequence of state transitions and events (see Figs. 4, 6 and 8; note that Fig. 8 shows an event log output to a display; see also column 4, lines 4-8, which shows that the timing of the events is considered as well) and a state table or matrix having coordinates for a display position (see column 9, lines 26-30).

Yamauchi further discloses the features of (d) above in terms of generating a test specification or script (see Fig. 24 and column 8, lines 55-62) based on a sequence of events and state transitions (see column 9, lines 11-14).

Yamauchi further discloses the features of (e) above in terms of outputting and displaying information based on each event in the state transition model as described in the test specification or script (see Fig. 25 and column 14, lines 14-25).

Yamauchi further discloses the features of (f) above in terms of converting a state transition model describing events and actions into a data structure, stored in memory, having event and state identification codes (see Fig. 3 and column 9, lines 11-39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

With respect to claim 4, Takuma does not disclose a script editor for editing said script file based on any one of an event input to be occurred, an occurrence timing of said event and an occurrence frequency.

Yamauchi further discloses the features above in terms of an editor for editing the test specification or script based on event inputs to occur (see Fig. 8 and column 10, lines 43-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

With respect to claim 5, the Takuma does not disclose the limitation wherein said script file is any one of a timing chart format, a text format and a message sequence chart format.

Yamauchi further discloses the features above in terms of a test specification or script that is in a text format (see Fig. 24 and column 14, lines 5-8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

With respect to claims 6, 7 and 8, Takuma further discloses the limitation wherein said program includes a main routine for executing a main process of said system and a normal

generating event routine for normally generating a corresponding event based on various data and a signal transmitted from said other component to said first central processing unit (see column 7, lines 37-50, which shows a processor having a routine for executing the instructions of a main monitor program and for responding to, i.e. generating events corresponding to, signals sent from a host processor).

With respect to claims 9, 10 and 11, Takuma does not disclose the limitation wherein said event pseudo-generating information is information of a generating technique in accordance with said event.

Yamauchi further discloses the features above in terms of a test sequence data structure, i.e. event pseudo-generating information, which comprises a sequential arrangement of events and actions (see column 9, lines 57-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

With respect to claims 12, 13 and 14, Takuma does not disclose the limitation wherein said event is any one of a message-type for receiving a start message from another task or another apparatus, a flag-type for reading a variation of a variable or an input/output, an interrupt-type for receiving an interrupt from an outside, an in-mail type for notifying an internal event which occurs in a cell of said state-transition matrix to another state-transition matrix when

said state-transition matrix is layered and a function-call type for calling a function executing a group of processes.

Yamauchi further discloses the features above in terms of events that are caused by external signals or interrupts (see column 3, lines 21-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the features taught by Yamauchi into the system of Takuma, for the purpose of enabling the testing of programs based on a plurality of events and state transitions (see Yamauchi, column 3, lines 62-67), which would further facilitate debugging (see Takuma, column 3, lines 33-36).

With respect to claim 15, see the explanation for claim 1 above. Note that claim 15 recites a program development method that is analogous to the program development apparatus recited in claim 1.

With respect to claim 16, see the explanation for claim 2 above. Note that claim 16 recites a program development method that is analogous to the program development apparatus recited in claim 2.

With respect to claim 17, see the explanation for claim 3 above. Note that claim 17 recites a program development method that is analogous to the program development apparatus recited in claim 3.

With respect to claim 18, see the explanation for claim 4 above.

With respect to claim 19, see the explanation for claim 5 above.

With respect to claims 20, 21 and 22, see the explanation for claims 6, 7 and 8 above.

With respect to claims 23, 24 and 25, see the explanation for claims 9, 10 and 11 above.

With respect to claims 26, 27 and 28, see the explanation for claims 12, 13 and 14 above.

With respect to claim 29, see the explanation for claim 1 above. Note that claim 29 recites a program development program that is analogous to the program development apparatus recited in claim 1.

With respect to claim 30, see the explanation for claim 1 above. Note that claim 30 recites a storage medium storing a program development program that is analogous to the program development apparatus recited in claim 1. Takuma further discloses a storage medium (see Fig. 2B, items 13, 40 and 80).

With respect to claim 31, see the explanation for claim 2 above. Note that claim 31 recites a program development program that is analogous to the program development apparatus recited in claim 2.

9. It is noted that claims 1-3, 15-17 and 26-28 are rendered obvious by Japanese Unexamined Patent Application Publication H12-020347 and Japanese Unexamined Patent Application Publication H5-324385, as shown in the Information Disclosure Statement filed on 28 October 2002 (Paper No. 4). The translated portion of the Korean Office Action shows that the cited inventions are "very similar in the aspects of constitution and effect [to the present invention], and other differences in constitution [are] no more than matters of choice which

could be selectively employed as necessary or which could be easily accomplished by simple circuit modification or combination by a person skilled in the art."

Cooperation is respectfully asked of applicant to provide full English translations of the foreign documents or an explanation as to how the present invention is not rendered obvious by the cited references.

10. It is noted that claims 1, 2, 6-10 and 14-17 are rendered obvious by the document "Maikon sofutouea yo togo CASE kankyo [Integrated CASE environment for microcomputer software]," as shown in the Information Disclosure Statement filed on 6 August 2003 (Paper No. 8). The translated portion of the Japanese Office Action shows that the cited literature is similar to the present invention.

Cooperation is respectfully asked of applicant to provide a full English translation of the foreign document or an explanation as to how the present invention is not rendered obvious by the cited reference.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Pat. No. 6,063,131 to Yoshida discloses an emulator system for program development. U.S. Pat. No. 5,978,584 to Nishibata et al. discloses a debugging system comprising an in-circuit emulator.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy
January 5, 2004

TUAN DAM
SUPERVISORY PATENT EXAMINER